

# Latency Hiding Strategies of Pre-Allocation Based Media Access Protocols for WDM Photonic Networks

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**Abstract** – Media access protocols that de-emphasize the performance impact of propagation delay, packet processing and switching latency for an optically star-coupled system with pre-allocated WDMA channels are introduced and compared. The channels are pre-allocated to the nodes with this approach, where each node has a *home channel* that it uses either for all data packet transmission or reception. A home channel may be shared if the number of nodes exceeds the number of channels in the system. This approach does not require both tunable transmitters and tunable receivers per node. Each node has a tunable transmitter and a fixed receiver plus a set of queues (one per channel) that are used to avoid head-of-line effects. The performance of a generalized random access protocol is compared to a protocol based on interleaved time multiplexing. Both protocols are designed to operate in a multiple-channel multiple-access environment and require each node to possess a tunable transmitter and a fixed (or slow tunable) receiver. The impact of network size, number of channels, transmitter tuning time, propagation delay and packet processing time on protocol design and performance is extensively studied.

## 1 INTRODUCTION

Pre-allocation media access protocols for *wavelength division multiple access* (WDMA) star-coupled photonic networks are investigated in this paper. Channels are allocated to nodes a priori in this approach reducing system complexity. Two pre-allocation protocols based on random (I-SA) and static (I-TDMA) access have been analyzed in [1] but propagation, protocol processing and optical device tuning times were not considered.

This paper considers protocol design in a more realistic scenario and develops overlapping techniques to reduce protocol sensitivity to propagation delay, optical device switching time and protocol processing time. Two protocols based on random access and static access with low implementational complexity are proposed and their performance compared.

A multiple access environment can be achieved through a variety of optical channel topologies [2]. Star-coupled networks have high fault-tolerance due to their passive nature and complete unity distance connectivity [3]. This high connectivity is achieved with low system complexity through the multiple access nature of the system. The protocols are described in terms of the star-coupled configuration due to its fanout characteristic and high network fault tolerance.

Media access control protocols developed for photonic star-

coupled WDM networks may be broadly classified into *reservation* and *pre-allocation* strategies [4]. *Reservation techniques* may designate one wavelength channel as the *control channel* that is used to reserve access on the remaining channels (designated as data channels) for data packet transmission [5, 6, 7, 8]. *Pre-allocation techniques* pre-assign the channels to the nodes, where each node has a *home channel* that it uses either for all data packet transmissions or all data packet receptions [9, 10, 3, 11, 1]. Pre-allocation achieves reduction in system complexity by eliminating the requirement of a control channel as discussed below.

The protocols defined in this paper are analyzed in terms of performance and also in terms of the following concerns.

The issues identified below are used throughout the paper to examine the suitability of the proposed protocols. In general, the problems are not new concerns but have taken on increased importance due to their relation with the transmission speed of optical networks:

**Propagation delay** – the time required for light energy to travel from source to destination.

The impact of propagation delay on performance is significant even for local area high-speed networks due to the reduced packet transmission time. This implies that acknowledgment based protocols may be vulnerable to severe performance degradation if this concern is not addressed. I-SA\*, a pre-allocation scheme introduced in this paper, is an acknowledgment based protocol that uses redundant acknowledgments and windowing to relax the propagation delay vulnerability.

The impact of variations in the ratio of propagation delay to nominal packet transmission time has been studied for optical bus-based demand assignment multiple access protocols in [2].

**Processing Latencies** – two main components of delay are the tuning latency of the optical devices and the latency of protocol overhead that cannot be overlapped or pipelined due to speed and cost constraints:

**Tuning Latency** – WDM networks usually require wavelength tunable transmitters and/or tunable receivers. The tuning latency of these optical devices is not negligible and has a significant impact on overall system performance.

In general, faster tuning requires higher cost. An objective of this work is to achieve more cost effective network solutions by developing techniques that perform well with slower devices by hiding the processing latencies.

**Packet Processing Overhead** – Incoming packets require opto-electronic conversion, header decoding and checksum

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verification. Outgoing packets require time to execute the protocol algorithm, to select the packet for transmission and to construct and append the header. Control channel based schemes face a difficulty since all packets transmitted on the control channel must be processed by all nodes. This places a very high demand, in terms of its throughput capability, on the receiver subsystem. Pre-allocation based schemes completely eliminate this requirement on the receiver subsystem by partitioning the data traffic for the different channels.

**Synchronization** – must be provided at both bit and frame levels.

The above discussion briefly compared reservation and pre-allocation in general terms. In particular, the motivation of the pre-allocation approach to remove the requirement of a control channel is described. The following sections examine the proposed protocols in terms of their sensitivity to propagation delay and processing latencies. The protocols do not have any additional advantage in terms of synchronization beyond the general benefit of pre-allocation that eliminates the requirement of a control channel.

The two pre-allocation protocols analyzed in [1] are based on random access (I-SA) and static access (I-TDMA). Both protocols assumed one tunable transmitter and one fixed receiver per node. Each node had a single queue of variable capacity which buffered packets that arrived while the transmitter was busy.

This paper generalizes I-SA and I-TDMA by incorporating  $C$  separate queues at each node where  $C$  is the number of channels in the system. The proposed protocols are referred to as I-SA\* and I-TDMA\* respectively. The main disadvantage of a single queue, as in I-SA and I-TDMA, is the head-of-line effect [1, 12] which can be eliminated in I-SA\* and I-TDMA\*.

Section 2 defines the two protocols. Section 3 analyzes the performance of the two protocols through discrete-event simulation models and compares their relative performance. The performance is evaluated in terms of system scalability (number of nodes and channels), propagation delay, packet processing time, transmitter switching latency and packet generation rate. Section 4 presents the conclusions.

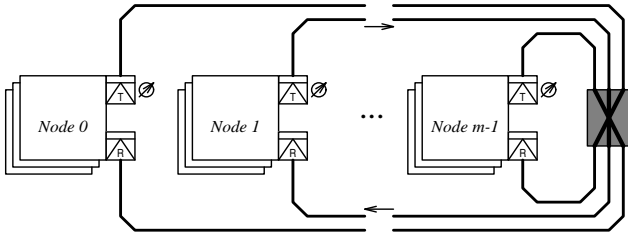


Figure 1: Network architecture for I-SA\* and I-TDMA\* with one tunable transmitter and a fixed (or slow tunable) receiver per node.

## 2 DESCRIPTION OF PROTOCOLS

The objective of pre-allocation is to avoid the requirement that each node possess both a tunable transmitter and a tunable receiver. Fig. 1 illustrates the network architecture used in this paper where each node has a tunable transmitter and a fixed or slow tunable receiver. The protocols are based on channels pre-allocated for data packet reception where each node receives on its home channel.

A source node tunes its transmitter to the home channel of the destination node and transmits according to the access protocol. Network traffic is partitioned so that each node does not have to

receive and process all transmitted packets. A node receives and processes only its home channel traffic. *Optical self-routing* is achieved when  $M = C$  since a home channel is not shared and a node receives traffic intended only for itself.

This paper considers two approaches for access arbitration of the target architecture. The first approach is random access based: access is based on Slotted Aloha (I-SA\*) where an idle source node tunes to the home channel of the destination node in the next slot following packet arrival and transmits the packet. The second approach statically allocates access in a time division fashion: access is based on Time Division Multiple Access (I-TDMA\*) where a source node transmits on the home channel of the destination node in the pre-assigned slot of the source node in the cycle immediately following packet arrival. The two protocols assume constant sized packets. Time is slotted and transmission is synchronized to packet boundaries.

Each node has a receiver which is tuned to its *home channel*. A source node can determine the home channel of the destination node in a decentralized fashion through the channel allocation policy [11, 10]. Let  $M$  and  $C$  denote the number of stations and channels, respectively. Node  $m_j$  is assigned  $c_i$  as its home channel based on an interleaved allocation policy where  $c_i = m_j \bmod C$ . Both protocols are denoted as I-X to show that they have an interleaved home channel allocation policy.

Each node has  $C$  separate queues, one per channel, of variable capacity. When a packet is generated, the channel on which this packet is to be transmitted is determined based on the destination and the allocation scheme. The packet is buffered in the corresponding channel queue if the transmitter is not available.  $C$  separate queues will avoid the head-of-line effects that severely degraded the performance of I-SA and I-TDMA [1, 13].

**Processing Latency:** Let  $T$  denote packet transmission time and  $\kappa$  denote the sum of protocol processing time and maximum transmitter tuning time between channels. Processing latency, denoted by  $\alpha$ , is defined as  $\alpha \triangleq \left\lceil \frac{\kappa}{T} \right\rceil$ .

**Propagation delay:** We assume that the network may not be symmetric so all nodes may not be equidistant from the star. Let  $\tau_i$  denote the propagation delay from node  $m_i$  to the star. Define  $\tau$  as the maximum node-to-star propagation delay given by  $\tau = \max\{\tau_i \mid 0 \leq i \leq M - 1\}$ , and normalized maximum propagation delay is denoted by  $a \triangleq \left\lceil \frac{2\tau}{t} \right\rceil$  where  $t$  is packet transmission time.

### 2.1 Interleaved Slotted Aloha (I-SA\*)

I-SA [1] is based on Slotted Aloha where a packet is transmitted in the next slot following its arrival. I-SA assumed a single queue of variable capacity per node. Collision occurs when more than one node transmits on the same channel. Successful packet transmissions could not be sensed by the source node since its receiver is tuned to its own home channel. The destination node has to indicate successful packet reception through an acknowledgment mechanism.

One way to accomplish acknowledgments is by extending the slot to include the acknowledgment. A packet slot is therefore composed of two phases: data transmission phase and acknowledgment phase which can be time division multiplexed among the nodes to avoid acknowledgment collisions. The source node knows about packet collision at the end of the packet slot in

which it was transmitted. The acknowledgment subplot includes destination node transmitter tuning time and propagation delay for the acknowledgment. One slot in I-SA is therefore equal to  $(2a + \alpha + 1)T$  time units where  $T$  is packet transmission time.

Channel utilization per slot is  $\frac{1}{2a + \alpha + 1}$ .

I-SA\* improves performance by providing  $C$  separate queues per node and requiring an explicit acknowledgment from the destination node eliminating the acknowledgment subplots. The slot length for I-SA\* is  $T$  time units in comparison to  $(2a + \alpha + 1)T$  for I-SA. The acknowledgment may be piggy-backed on outgoing packets or transmitted in an empty packet (forced acknowledgment).

The data packet is composed of header fields and data field (which is empty in a forced acknowledgment). The header contains the source-destination pair, packet sequence number and piggy-backed acknowledgments:

*sender*: the source node of the packet.

*receiver*: the destination node of the packet.

*home channel*: the home channel of the source node.

*sequence number*: each node maintains a per channel sequence number incremented for each transmitted packet.

*acknowledgments*: The acknowledgment field contains acknowledgments for each node that will receive this packet. The acknowledgment mechanism is explained in the following paragraphs.

### 2.1.1 Redundant Acknowledgments

The primary objective of redundant acknowledgments is to reduce the latency in returning the acknowledgment in an environment with collisions. This approach to reduce the latency is to acknowledge successful packet transmission rather than successful packet reception. This allows the acknowledgment mechanism of I-SA\* to be consistent with collisionless TDM-based protocols such as I-TDMA\*. Due to finite receiver buffering at a node, a packet may be dropped even with a collisionless protocols (such as I-TDMA\*). A source node knows that its packet was successfully transmitted but can not be certain that its packet was successfully received at the destination. This implies that transport level acknowledgments are still required although media access level acknowledgments may not be needed (as with I-TDMA\*).

All packets successfully transmitted on a channel are received and decoded by all nodes which share the home channel. The header field of a packet is examined at each node to determine the destination and access the acknowledgment field. A node will discard a received packet if it was not the intended destination but will use the information obtained by acknowledgment field to update its local tables (described below). This allows a source node to acknowledge all nodes who share a home channel with a single packet rather than only acknowledging the specific destination node. This redundancy of acknowledgments reduces unnecessary retransmissions due to lost acknowledgments.

Each node maintains the status of packets transmitted by the node and packets received successfully from other nodes through the following tables: (i) Timer: retransmission timer per channel – data is allowed to be transmitted on the channel after this timer reaches zero; (ii) ACK: sequence number of first unacknowledged packet on a channel; and (iii) LPR: sequence number of last packet successfully received from all other nodes. The timer table is

updated by the transmitter. The ACK and LPR tables are updated by the receiver.

Let  $H_k$  denote the set of nodes sharing home channel  $c_k$  for all  $0 \leq c_k \leq C - 1$ . Suppose node  $m_s$  (with home channel  $c_s$ ) transmits on channel  $c_k$  to destination node  $m_d$ . The packet contains acknowledgments for all nodes in set  $H_k$ . For each node  $m_{k_1} \in H_k$ , the acknowledgment information for that node is composed from the LPR table of node  $m_s$ . Source node  $m_s$  thus transmits acknowledgments to all nodes in set  $H_k$  through a single packet. This makes use of the multicast capabilities of the pre-allocation approach. Determining the members of  $H_k$  is a simple operation based on the allocation policy.

If the packet is successfully transmitted, all nodes in set  $H_k$  decode the header information as discussed above. HeaderACK[ $m_{k_1}$ ] denotes the decoded acknowledgment information for node  $m_{k_1}$ ; and ACK[ $c_s$ ] denotes the ACK table entry of node  $m_{k_1}$  for channel  $c_s$ . HeaderACK[ $m_{k_1}$ ] > ACK[ $c_s$ ] indicates that more packets transmitted by node  $m_{k_1}$  on channel  $c_s$  have been successful. Node  $m_{k_1}$  updates its local ACK table entry and removes acknowledged packets from the buffer. It also updates its local LPR table to mark this successfully transmitted packet from node  $m_s$  on channel  $c_k$ . The rule for updating this table is described in Section 2.1.3. Since all nodes in set  $H_k$  perform this action, acknowledgment information is replicated among these nodes without incurring additional overhead.

I-SA\* takes advantage of channel pre-allocation and reduces the number of acknowledgments by providing simultaneous feedback to all nodes sharing a home channel. Furthermore, since an acknowledgment may be lost due to collision, I-SA\* eliminates unnecessary retransmissions by replicating acknowledgment information among nodes sharing a home channel. These features attempt to reduce the impact of acknowledgments on the performance of I-SA\*.

Protocol behavior can be described by describing the transmitter and receiver behavior during each time slot. The system changes state only at the beginning of a time slot. The following sections describe the protocol in further detail.

### 2.1.2 Transmitter

At the beginning of each slot the transmitter may transmit data or a forced acknowledgment packet or remain idle for the remainder of the slot.

1. Packet availability in the queues is indicated in a  $C$ -bit register. If a queue is not empty and the channel timer (explained below) is zero the corresponding bit is set. Ideally, the queues can be examined in a random order to ensure fairness among all queues. One practical way to achieve this is to examine the queues in a revolving cyclic ordering.
2. In the order chosen in Step 1 the first queue which has a valid packet is selected. A queue is said to have a valid packet if the channel timer has expired and there is an unacknowledged or new packet in the queue.  
Step 3 is skipped if none of the queues have a valid packet and Step 4 is skipped if the transmitter decides to transmit.
3. The transmitter tunes to the channel corresponding to the selected queue and transmits a window of packets or until the queue is empty. If a packet is acknowledged in the tuning interval, the next available packet is transmitted. Acknowledgment information is piggy-backed onto each data packet. After transmitting the last packet, the channel timer is set (this value is obtained from the source timeout parameter described below). Packets are not transmitted on this channel until the timer is reset to zero. The window of packets is used to de-emphasize tuning latency and propagation delay.

4. A forced acknowledgment is transmitted if a packet targeted to this node has not been acknowledged. If more than one packet is to be acknowledged, a round-robin scheme as described in Step 1 is used to select the channel.

When a packet is unacknowledged after the timeout expires, the node follows a backoff policy to decide retransmission. This paper assumes a geometric distribution with parameter  $\eta$  for backoff. The transmitter uses a *Go-Back-N* policy in case of packet collisions where all packets in the window are retransmitted starting from the collided packet. This eliminates the need for buffer resequencing at the destination node as with Selective Repeat.

### 2.1.3 Receiver

The receiver continuously updates status tables with information about packets received from other nodes. Since the receiver is parked at the home channel of the node, it receives all packets that are successfully transmitted on this channel. The receiver performs the following operations if the transmission in the previous slot was not a collision. The receiver does not update any of the status tables upon collision.

1. The packet is decoded and the local acknowledgment table is updated from the acknowledgment fields of the packet. Acknowledged packets and all packets preceding it are removed from the queue. *Sliding window* control is used since each channel window moves forward only after receiving an acknowledgment. This ensures flow control on each channel and provides fair transmitter access to all channel queues.
2. At each node, LPR[i] contains the highest sequence number received from node  $i$ . Let  $S_i$  denote the sequence number of the incoming packet. If  $S_i = \text{LPR}[i] + 1$ , the packet is in sequence and the LPR entry is updated.

If the packet is intended for this node and is in correct sequence, it is transferred to the data processing unit. Packets received out of order are discarded.

The goal is to keep the receiver algorithm simple so the transmitter has the updated information about the previous slot before transmitting in the current slot.

### 2.1.4 Design Parameters

The configuration of I-SA\* is determined by a set of system and design parameters. The system parameters are number of channels ( $C$ ), number of nodes ( $M$ ), propagation delay ( $a$ ), processing latency ( $\alpha$ ) and mean packet generation rate per node ( $\lambda$ ). The design parameters ( $l$ ,  $A$  and  $W$ ) are explained below.

**Source Timeout:** After transmitting the last packet in a window, the node defers transmission on a channel until the channel timer expires or until all the packets in the window have been acknowledged. The channel timer is set to  $2a + \alpha + l$  slots where  $l$  is the source timeout parameter. The transmitter retransmits all the packets in the window starting from the first collided packet. The value of  $l$  is determined based on the probability of success.

**Destination Timeout:** The time interval between packet reception and forced acknowledgment transmission is denoted by  $A$ . Under light input traffic, the destination transmits a forced acknowledgment since the source node may retransmit the same packet due to a lack of acknowledgments. At higher loads, piggy-backed acknowledgments used increase in frequency and

forced acknowledgment is not needed. Setting  $A$  to large values encourages piggy-backed acknowledgments.

$l$  and  $A$  may be fixed or dynamic, varying with system load and probability of success. This paper assumes a fixed  $l$  and  $A$ .

**Window Size:** One possible solution to reduce the impact of transmitter switching latency, protocol processing time and propagation delay is to reduce the average packet switching time and the amount of work that can be performed per switch. This can be accomplished by transmitting a window of packets after tuning to a channel. The window size is denoted by  $W$  and a *Go-back-N* policy is used for packet retransmission where  $N = W + 1$ . As with  $l$  and  $A$ ,  $W$  can be fixed or dynamic.

### 2.1.5 Addressing Network Design Issues

In this section, we examine the effectiveness of I-SA\* in handling the issues discussed in Section 1.

**Propagation Delay:** I-SA\* is based on acknowledgments and is sensitive to propagation delay, tuning time and packet processing time. A packet is acknowledged after at least  $2a + \alpha + 1$  time units after transmission. The impact of propagation delay and transmitter tuning time for the acknowledgment is reduced by overlapping source timeout with propagation delay and the window approach. The node is able to transmit on other channels while acknowledgment is awaited from other destination nodes. **Processing Latency:** I-SA\* reduces the average switching time per packet by allowing a window of packets to be transmitted after tuning to a channel. This attempts to reduce the processing overhead per packet.

## 2.2 Interleaved TDMA (I-TDMA\*)

Collisions can occur during packet transmission of I-SA\* as described above requiring packet retransmission which increases packet delay and decreases system throughput. The protocol defined in this section avoids collisions and the complexity of supporting acknowledgments and retransmissions by time multiplexing access to the destination nodes. I-SA\* is also sensitive to propagation delay since acknowledgments are required. I-TDMA\* renders itself insensitive to propagation delay by eliminating acknowledgments at the media access level.

Time is slotted on each channel and the home channels are pre-allocated for packet reception. Every node in the system has a chance to transmit to a destination node on each channel per cycle. A cycle, denoted by  $\mathcal{L}$ , is defined as the length of time required to allocate permission for all nodes to transmit on all channels. The minimum cycle length is  $\mathcal{L} = M$  if  $C < M$ . Minimum cycle length is  $\mathcal{L} = M - 1$  for  $C = M$  if we assume a node does not transmit to itself.

I-TDMA\* is similar to I-TDMA [1] except that each node has  $C$  queues of variable capacity – one per channel. Packets are buffered in the corresponding channel queue. I-TDMA\* is collision free because the channel allocation scheme ensures that only one node is allowed to transmit on the same channel at the same time.

A node requires  $T = \alpha + 1$  time units to transmit a packet on a channel and a total of  $CT$  time units to transmit on all channels. The allocation schemes vary with  $C$ ,  $M$  and  $T$ . and are denoted by I-TDMA<sub>0</sub>\*, I-TDMA<sub>1</sub>\* and I-TDMA<sub>2</sub>\*. The cycle length for the schemes is  $M$ ,  $CT$  and  $M$  respectively. The three schemes are described in detail below.

I-TDMA<sub>0</sub>\*: This scheme is used when  $CT \leq M$  and cycle length in this scheme is  $\mathcal{L} = M$  for  $C < M$ . If we assume a node does not transmit to itself,  $\mathcal{L} = M - 1$  for  $C = M$ . The transmitter is active for  $CT$  slots and idle for  $M - CT$  slots in each cycle. However, all slots are utilized in each cycle. Performance is not degraded for all values of  $\alpha$  which satisfy the condition  $CT \leq M$  since switching is completely overlapped with cycle synchronization.

The allocation scheme is described as follows. Node  $m_i$  is initially allocated channel  $c_0$  at time  $((i + 1) \bmod M)$ . Subsequent channels are allocated  $T$  units apart until all channels are allocated for this cycle. The node remains idle for  $M - CT$  slots after which channel 0 is allocated again. Since channels are allocated  $T$  units apart, the transmitter tunes to the next channel in this interval and a packet can be transmitted immediately without further tuning delay in the allocated slot.

Under light traffic, the average delay is  $M/2$  slots irrespective of  $\alpha$  and this includes cycle synchronization delay. Under heavy traffic, every node has a packet to transmit on each channel. Each slot of the cycle is utilized and maximum system throughput  $\mathcal{S}_{max} = C$  is achieved under extreme load conditions. System throughput is defined as the number of packets transmitted per slot across all  $C$  channels.

If  $CT > M$ , two ways of designing the allocation scheme are considered next. The first is an extension of I-TDMA<sub>0</sub>\* and results in an extended cycle. The second scheme retains the cycle length as  $M$  losing interleaving as a trade-off.

I-TDMA<sub>1</sub>\*: This allocation scheme is an extension of I-TDMA<sub>0</sub>\* described above. The cycle is extended to allocate permission for each node to transmit on all channels and  $\mathcal{L} = CT$ . Subsequent channels are allocated to a node  $T$  units apart as before. Transmitter tuning is overlapped with cycle synchronization and average packet delay under light traffic is  $\mathcal{L}/2$ . Note that this delay is only due to cycle synchronization and there is no tuning delay. Only  $M$  out of  $\mathcal{L}$  time slots per channel cycle are utilized for data transmission. Maximum per channel utilization is therefore  $\frac{M}{\mathcal{L}}$  and hence maximum system throughput is given by  $\mathcal{S}_{max} = \frac{M}{T}$ .

The allocation map is identical to I-TDMA<sub>0</sub>\* except that the cycle length is  $CT$ . Node  $m_i$  is initially allocated channel  $c_0$  at time  $((i + 1) \bmod \mathcal{L})$  and subsequent channels are allocated  $T$  units apart. This scheme wastes slots; it is a tradeoff to retain a simple allocation scheme.

I-TDMA<sub>2</sub>\*: The cycle length is retained as  $M$  in this scheme. After transmitting a packet on channel  $c[j, i]$  during slot  $i$ , node  $m_j$  begins tuning to channel  $c[j, 1 + (i + \alpha) \bmod (M)]$  if its transmit buffer for this channel is non-empty. The slots between  $i$  and  $1 + (i + \alpha) \bmod (M)$  are not used and are lost since there must be at least  $\alpha$  slots between consecutive transmissions.

Note that if  $x(\alpha + 1) = M$  for some positive integer  $x$ , an extra slot must be skipped when cycle boundaries are crossed so the same set of channels is not visited each cycle to retain fairness.

This scheme works better than I-TDMA<sub>1</sub>\* under light traffic since cycle length is  $M$  compared to  $CT$  for I-TDMA<sub>1</sub>\*. The average delay at lighter loads is  $\alpha + \frac{M}{2}$  with I-TDMA<sub>2</sub>\* and  $\frac{CT}{2}$  with I-TDMA<sub>1</sub>\*.

At higher traffic rates when queues are always full, a node can transmit at most  $\left\lceil \frac{C}{T} \right\rceil$  packets per cycle since each packet requires  $T$  time units. Maximum system throughput is therefore

$\mathcal{S}_{max} = \left\lceil \frac{C}{T} \right\rceil$  for  $C < M$ . I-TDMA<sub>1</sub>\* and I-TDMA<sub>2</sub>\* have identical maximum throughput of  $\frac{M}{T}$  when  $C = M$ . In this case, I-TDMA<sub>2</sub>\* has an advantage over I-TDMA<sub>1</sub>\* because of its smaller cycle length.

## 2.2.1 Addressing Network Design Issues

I-TDMA\* offers the advantages of using a pre-allocation strategy as explained in Section 2.1.5 – receiver processing and bit synchronization. In this section, we consider the impact of propagation delay and transmitter tuning time.

**Propagation Delay:** A significant advantage of I-TDMA\* is that it is not dependent on acknowledgments and is **not** sensitive to propagation delay since transmissions are collision free. The only effect of propagation delay on performance is the linear increase in delay. This cannot be avoided because of physical limitations.

**Processing latency:** The interleaved allocation of I-TDMA<sub>0</sub>\* completely eliminates the impact of  $\alpha$  if I-TDMA<sub>0</sub>\*. The impact of  $\alpha$  is not completely eliminated for higher values of  $\alpha$  but alternate schemes have been provided to overlap channel tuning with cycle synchronization.

## 3 ANALYSIS OF PERFORMANCE METRICS

This section analyzes I-SA\* and I-TDMA\* through discrete-event simulation models. Refer to [1, 7] for a description of an analytic technique based on semi-markov models that accurately portrays both reservation and pre-allocation protocols. Analytic models were not found to provide additional insight into protocol performance and are not considered in this paper.

The performance metrics of interest are average packet delay and network throughput. The impact of varying packet generation rate ( $\lambda$ ), number of nodes ( $M$ ), number of channels ( $C$ ), processing latency ( $\alpha$ ) and propagation delay ( $a$ ) is analyzed.

**Packet Delay:** denoted by  $\mathcal{D}$  is defined as the time elapsed between the generation of the packet and the time its acknowledgment is received at the source node. In I-TDMA\*, where there are no acknowledgments, packet delay is defined as the time elapsed between packet generation and transmission completion.

**Network Throughput:** denoted by  $\mathcal{S}$  is defined as the number of packets that are successfully transmitted per slot across all channels. Since there are  $C$  channels in the system, the maximum network throughput is  $C$ . Maximum network throughput which is achieved under extreme load is denoted by  $\mathcal{S}_{max}$ .

### 3.1 Simulation Model

The simulators are based on stochastic self-driven discrete event models, written in the  $C$  programming language with SimPack. SimPack is a  $C$  based library of routines that provides discrete-event and random variate facilities. Steady state transaction times and throughput were measured. Simulation convergence was obtained through the replication/deletion method [14], with a 99% confidence in a less than 2% variation from the mean for I-TDMA\*. The results for I-SA\* converged with a 95% confidence in a less than 5% variation from the mean.

The simulation model makes use of the following assumptions: (i) All nodes are independent of each other and identical; (ii) Packet generation at each node follows a Poisson process with a rate of

$\lambda$  packets per unit time per node; (iii) A packet generated at node  $m_i$  is targeted to node  $m_j$  with probability  $\frac{1}{M-1}$  for  $i \neq j$ ,  $0 \leq i \leq M-1$  and  $0 \leq j \leq M-1$ ; and with probability 0 when  $i = j$  (Uniform Reference Model); (iv)  $C$  packet queues of variable capacity – one per channel. In this paper, the queues have unlimited capacity; and (v) All packets are of fixed length.

### 3.2 Performance of I-TDMA\*

The performance of I-TDMA\* is analyzed in this section. It was noted earlier that propagation delay results in a linear increase in delay which is inevitable and does not affect capacity. The following graphs have been plotted for  $a = 0$ .

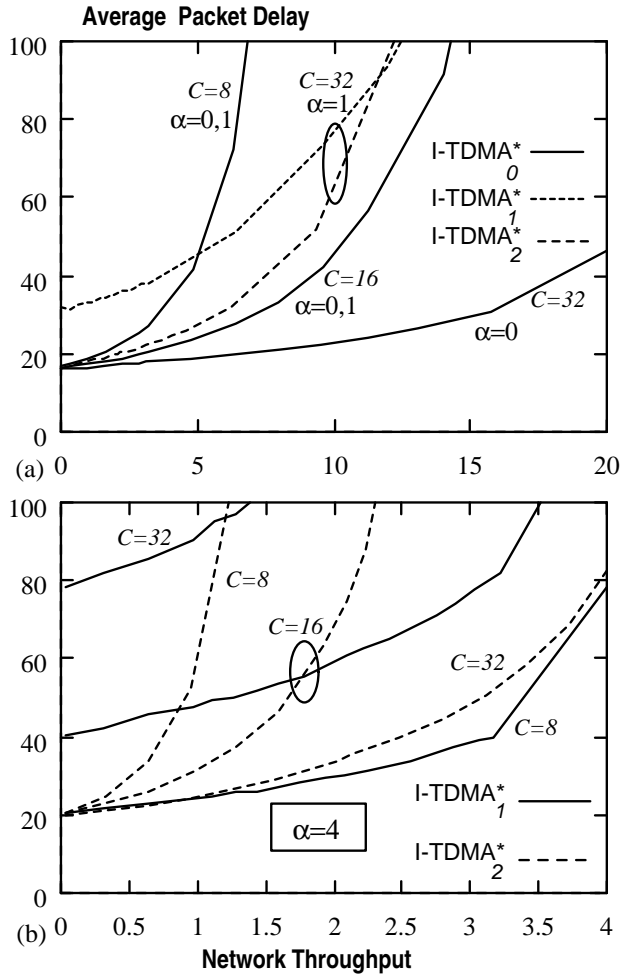


Figure 2: Performance of I-TDMA\* for  $M = 32$ ,  $C \in \{8, 16, 32\}$  and  $\alpha \in \{0, 1, 4\}$ : (a)  $\alpha \in \{0, 1\}$  (b)  $\alpha = 4$ .

#### 3.2.1 Scalability in Channels

Fig. 2 shows the performance impact of varying  $C$  for  $M = 32$  and  $\alpha \in \{0, 1, 2, 4\}$ . In general, increasing the channels should improve performance. Fig. 2(a) shows the effect of increasing the number of channels for  $\alpha \in \{0, 1\}$ . For  $\alpha = 0$ , the relation

$CT \leq M$  holds for all values of  $C$  since  $C \leq M$  and  $\mathcal{L} = M$ .  $\mathcal{D}$  reduces with increasing  $C$  and in each case,  $\mathcal{S}_{max} = C$ . The decrease in  $\mathcal{D}$  at  $\mathcal{S} = 5$  is 50% when  $C$  is increased from 8 to 32 for  $M = 32$  and  $\alpha = 0$ .

For  $\alpha > 0$  the time spent switching between channels affects the cycle length and hence the performance. Increasing the number of channels also increases the total switching time in one cycle. The performance improves with increasing  $C$  until  $C = C_{opt}$  where  $C_{opt}$  is the value of  $C$  that provides maximum performance and is given by  $C_{opt} = \lfloor M/T \rfloor$ .  $\mathcal{S}_{max} = C$  if  $C \leq C_{opt}$ .  $C_{opt}$  decreases with increasing  $\alpha$ . If  $C_{opt} < C < M$ , then  $\mathcal{S}_{max} = M/T$  for I-TDMA\*<sub>1</sub> and  $\mathcal{S}_{max} = \lceil C/T \rceil$  for I-TDMA\*<sub>2</sub>. For  $C = M$ , is  $\mathcal{S}_{max} = M/T$  for both schemes.

Fig. 2(a) shows the effect of increasing  $C$  for  $M = 32$  and  $\alpha = 1$ . The performance improves with increasing  $C$  until  $C = C_{opt}$  where  $C_{opt} = 16$  for  $M = 32$  and  $\alpha = 1$ . For  $C > 16$ ,  $\mathcal{D}$  of I-TDMA\*<sub>1</sub> increases with  $C$  due to the extended cycle and  $\mathcal{S}_{max}$  is limited to 16. I-TDMA\*<sub>2</sub> results in lower delay under light traffic but  $\mathcal{S}_{max}$  is limited to  $\lceil C/2 \rceil$ .

Fig. 2(b) shows the effect of increasing  $C$  for  $\alpha \in \{2, 4\}$ .  $C_{opt} = 6$  for  $\alpha = 4$ .  $\mathcal{D}$  is lower under light traffic for I-TDMA\*<sub>2</sub> but I-TDMA\*<sub>1</sub> has higher capacity.  $\mathcal{S}_{max}$  with both schemes is 6 for  $\alpha = 4$ .

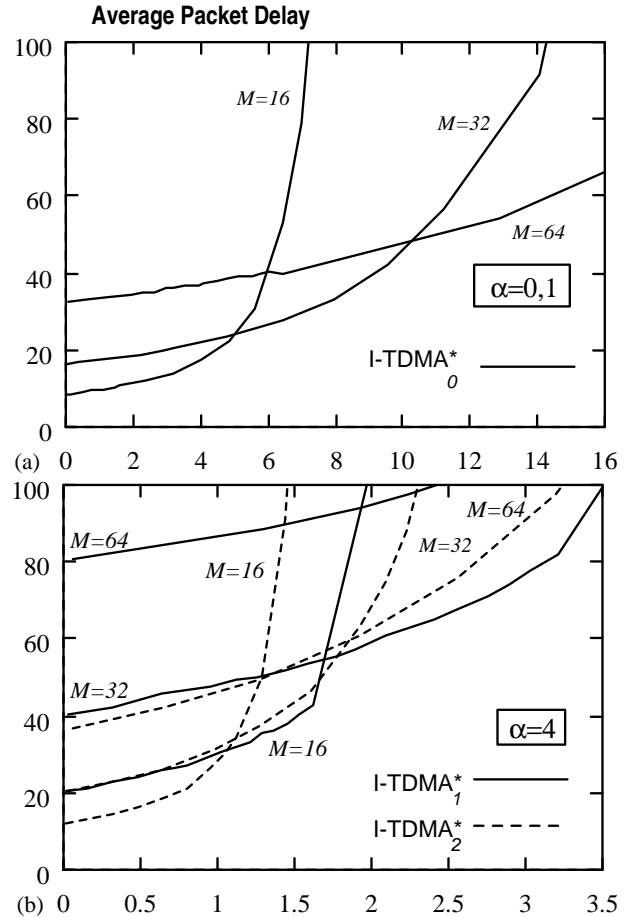


Figure 3: Performance of I-TDMA\* varying  $M$  for  $C = M/2$  and  $M \in \{16, 32, 64\}$ : (a)  $\alpha \in \{0, 1\}$  (b)  $\alpha = 4$ .

### 3.2.2 Scalability in System Size

Fig. 3 plots performance with variations in system size for  $M \in \{16, 32, 64\}$ ,  $C = M/2$  and  $\alpha \in \{0, 1, 2, 4\}$ . If  $CT \leq M$ , the cycle length is equal to  $M$  and average delay increases with increasing  $M$  but is independent of  $\alpha$ . Fig. 3(a) plots the performance for  $\alpha \in \{0, 1\}$  where  $CT \leq M$  and shows that the performance is identical for both values of  $\alpha$ .  $\mathcal{D}$  under light traffic is approximately  $M/2$  due to the synchronization delay.  $S_{max} = C$  for all values of  $M$  presuming that  $C \leq M$ .

Fig. 3(b) plots the performance with both schemes for  $\alpha = 4$  where  $CT > M$ . Packet delay is dependent on  $C$  and  $T$  for I-TDMA<sub>1</sub><sup>\*</sup> and dependent on  $M$  for I-TDMA<sub>2</sub><sup>\*</sup>. However, since  $C = M/2$ ,  $\mathcal{D}$  is seen to increase with  $M$  for both schemes.  $S_{max} = M/5$  with I-TDMA<sub>1</sub><sup>\*</sup> and  $M/10$  with I-TDMA<sub>2</sub><sup>\*</sup> showing that the former scheme has higher system capacity for  $C < M$ .

Given  $C$  and  $\alpha$ ,  $M_{min}$  is defined as the minimum number of nodes that satisfies the condition  $CT \leq M$ . If  $M \geq M_{min}$ ,  $\mathcal{L} = M$  and  $S_{max} = C$ . If  $M < M_{min}$ ,  $\mathcal{L} = CT$  for I-TDMA<sub>1</sub><sup>\*</sup> and  $\mathcal{L} = M$  for I-TDMA<sub>2</sub><sup>\*</sup>.  $S_{max} = M/T$  and  $S_{max} = \lceil C/T \rceil$  respectively for the two schemes.

### 3.3 Performance of I-SA\*

This section describes the performance of I-SA\* and examines the effect of the system parameters ( $C$ ,  $M$ ,  $a$  and  $\alpha$ ), and the design parameters ( $l$ ,  $A$  and  $W$ ). Packet delay in I-SA\* is defined as the time between packet generation and acknowledgment arrival at the source node. The first set of graphs study the effect of varying parameters for  $W = 1$  to be consistent in comparison with I-TDMA\*. The effect of varying  $W$  on protocol performance is then analyzed.

In the following discussion,  $l = 16$  and  $A = 16$  where these values have been empirically chosen since they provided maximum throughput for the cases studied. However,  $\mathcal{D}$  under light traffic is higher since average delay under light traffic is given by  $2a + 2T + A$ .

#### 3.3.1 Scalability in Channels

Fig. 4 shows the effect of varying the number of channels for  $M = 32$ ,  $\alpha \in \{0, 1, 2, 4\}$ ,  $l = 16$ ,  $A = 16$  and  $W = 1$ . Increasing  $C$  reduces the number of collisions due to reduced traffic directed to each channel. This increases system throughput and decreases packet delay.

Fig. 4(a) shows the performance improvement obtained by increasing  $C$  for  $\alpha = 0$ . The average delay is identical for all values of  $C$  at lower loads due to negligible collision probability. The system capacity increases significantly as  $C$  increases.  $S_{max}$  increases by 175% when  $C$  increases from 4 to 32 for  $M = 32$  and  $\alpha = 0$ .  $\mathcal{D}$  for  $M = 32$  and  $\alpha = 0$  reduces by 200% as  $C$  increases from 4 to 32 at  $\mathcal{S} = 1$ . Fig. 4(a) also shows the performance improvement obtained by increasing  $C$  for  $\alpha = 1$ . The effect of increasing  $C$  is identical to that observed for  $\alpha = 0$ .

The performance gain diminishes with increasing  $\alpha$  due to increased switching overhead with increasing  $C$ . Fig. 4(b) shows the reduction in performance improvement for  $\alpha = 2$  and  $\alpha = 4$ . The increase in  $S_{max}$  obtained by increasing  $C$  from 4 to 32 for  $M = 32$  and  $\alpha = 4$  is 44% compared to 175% for  $\alpha = 0$ . Similarly, the decrease in  $\mathcal{D}$  when  $C$  is increased from 4 to 32 is 115% at  $\mathcal{S} = 1$  for  $M = 32$  compared to a 200% decrease for  $\alpha = 0$ . An increase in  $C$  thus results in improved performance but the magnitude of improvement diminishes for higher  $\alpha$ .

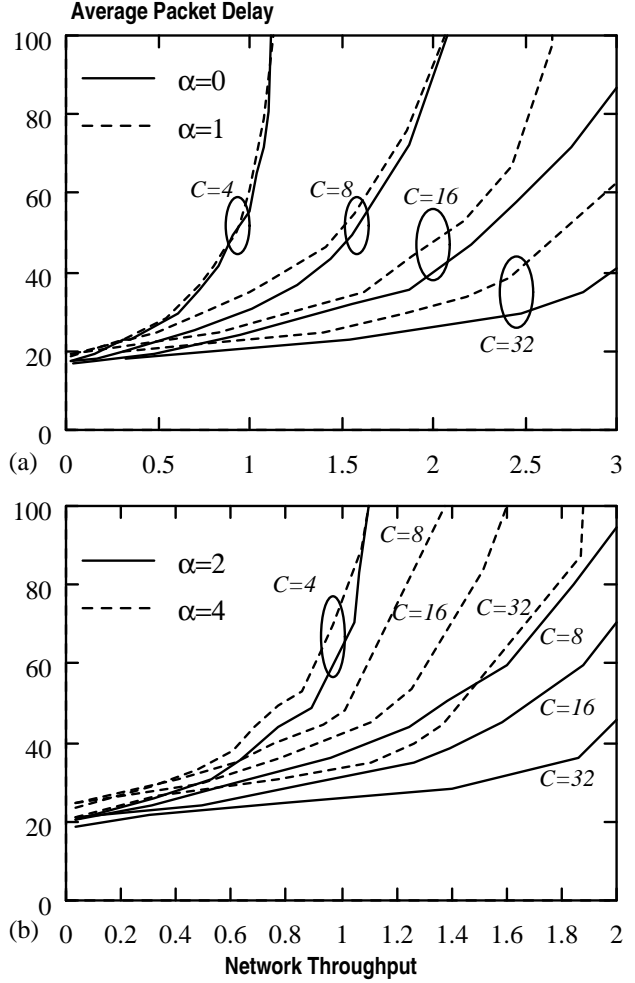


Figure 4: Performance of I-SA\* with varying  $C$  for  $C \in \{4, 8, 16, 32\}$ ,  $M = 32$ ,  $l = 16$ ,  $A = 16$  and  $W = 1$ : (a)  $\alpha \in \{0, 1\}$ , (b)  $\alpha \in \{2, 4\}$ .

#### 3.3.2 Scalability in System Size

Fig. 5(a) shows the impact of varying  $M$  on average packet delay and Fig. 5(b) shows the effect on network throughput for  $M \in \{16, 32, 64\}$ ,  $C = M/2$ ,  $\alpha \in \{0, 4\}$ ,  $l = 16$ ,  $A = 16$  and  $W = 1$ . It was shown in [1] that I-SA was scalable in that the delay characteristics were maintained with increasing  $M$  so long as the ratio  $M/C$  was constant. This is not observed in I-SA\* as seen from Fig. 5(a). However, network throughput increases with  $M$  since more nodes contribute more traffic to the system.

System traffic increases with increasing  $M$  thereby reducing probability of success. However, if the ratio  $M/C$  is maintained so that the amount of traffic directed to a channel is constant, delay characteristics can be maintained. This scalability is observed in I-SA. In I-SA\*, increasing  $M$  increases delay even if the ratio  $M/C$  is kept constant.  $\mathcal{D}$  at  $\lambda = 0.08$  increases by 50% when  $M$  was increased from 16 to 64 for  $C = M/2$  and  $\alpha = 0$ . This can be attributed to the explicit acknowledgment required by I-SA\* which increases system traffic. The size of status table LPR (Section 2.1) increases with  $M$  and the acknowledgment traffic is

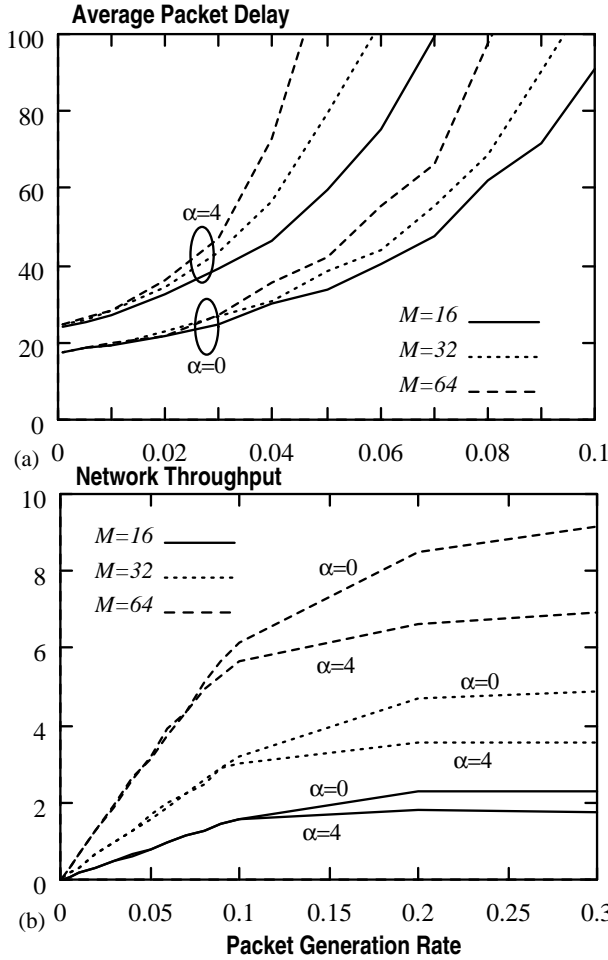


Figure 5: Performance of I-SA\* with varying  $M$  for  $M \in \{16, 32, 64\}$ ,  $C = M/2$ ,  $\alpha \in \{0, 4\}$ ,  $l = 16$ ,  $A = 16$  and  $W = 1$ : (a) Average Packet Delay (b) Network Throughput.

consequently higher. Fig. 5(a) also shows the effect of varying  $M$  for  $\alpha = 4$ . The discussion above holds true for  $\alpha = 4$  where increased acknowledgment traffic impacts the scalability of the protocol. For example,  $\mathcal{D}$  at  $\lambda = 0.8$  increases by 60% when  $M$  is increased from 16 to 64 for  $C = M/2$  and  $\alpha = 4$ .

Network throughput increases with  $M$  since more nodes contribute more traffic as seen in Fig. 5(b). However, more nodes increases the probability of packet collisions. The graphs show that so long as the ratio  $M/C$  is maintained, impact of  $\alpha$  on network throughput is negligible until saturation. Beyond saturation, throughput decreases with increasing  $\alpha$ . Note that the saturation point is roughly the same at  $\lambda = 0.1$  for all values of  $M$  and  $\alpha$  as long as ratio  $M/C$  is constant.

### 3.3.3 Impact of Propagation Delay and Processing Latencies

This section examines the behavior of I-SA\* with variations in the propagation delay and processing latencies, and then investigates how the windowing approach and the de-coupled redundant acknowledgment scheme can be used to hide the performance

degradation.

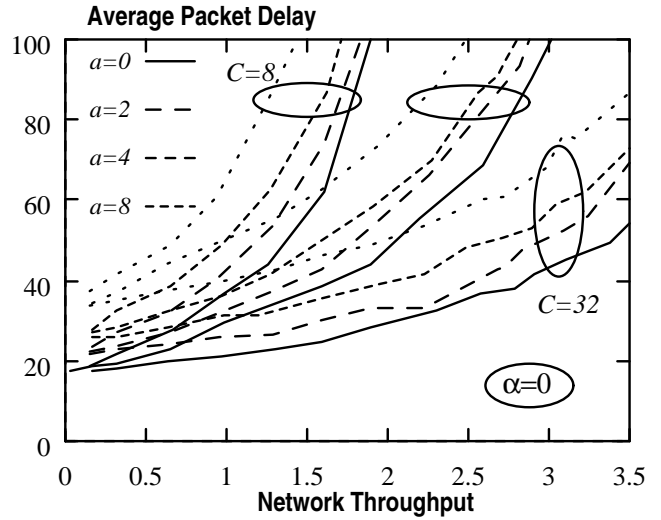


Figure 6: Performance of I-SA\* with varying  $a$  for  $C \in \{8, 16, 32\}$ ,  $M = 32$ ,  $\alpha = 0$ ,  $a \in \{0, 2, 4, 8\}$ ,  $l = 16$ ,  $A = 16$  and  $W = 1$ .

**Propagation delay:** Fig. 6 shows the effect of propagation delay for  $C \in \{8, 16, 32\}$ ,  $M = 32$ ,  $\alpha = 0$  and  $a \in \{0, 2, 4, 8\}$ . I-SA\* is sensitive to propagation delay because it is dependent on acknowledgments. The source node will wait for at least  $2a + \alpha + 1$  units for the acknowledgment before timeout occurs. However, the node can transmit on other channels rather than wait for an acknowledgment as explained earlier.

Increasing  $a$  results in increased packet delay for all values of  $C$  as seen from Fig. 6. Packet delay at  $\mathcal{S} = 1.3$  increases by 90% for  $C = 8$  and  $M = 32$  when  $a$  increases from 0 to 8.  $\mathcal{D}$  increases by at least  $2a$  due to acknowledgment waiting time and longer queuing delays at the source node is also observed. Similarly, for  $C = 32$  and  $M = 32$ ,  $\mathcal{D}$  at  $\mathcal{S} = 3$  increases by 70% when  $a$  increases from 0 to 8. In general, the impact of  $a$  does not seem to vary with varying  $C$ . Network throughput decreases in all cases due to the longer time spent by a packet in the queue. However, the decrease in maximum throughput is less than 10% for all cases when  $a$  is increased from 0 to 8.

**Processing latencies:** Fig. 7 shows the effect of varying  $\alpha$  for  $C \in \{8, 32\}$ ,  $M = 32$ ,  $l = 16$ ,  $A = 16$  and  $W = 1$ . Increasing  $\alpha$  increases the active time per packet of the transmitter since  $T = \alpha + 1$ . This increases packet delay and reduces system throughput. As  $\alpha$  increases, increased processing overhead results in lower transmitter utilization.

Fig. 7 shows the effect of increasing  $\alpha$  for  $C = 8$  and  $M = 32$ .  $S_{max}$  reduces by 28% and  $\mathcal{D}$  at  $\mathcal{S} = 1.4$  increases by 43% when  $\alpha$  increases from 0 to 4 for  $C = 8$  and  $M = 32$ . The impact of  $\alpha$  is to be higher for larger  $C$  as seen from Fig. 7 for  $C = 32$  and  $M = 32$ . This is due to the increased sensitivity to switching overhead since the overlap is decreased. A node does not hold a channel during the  $\alpha$  processing time so it could be used by some other node for transmission thereby overlapping the processing latency. The likelihood of this occurring decreases as  $C$  increases.  $S_{max}$  reduces by 60% and  $\mathcal{D}$  at  $\mathcal{S} = 1.5$  increases by 200% for  $C = 32$  and  $M = 32$  when  $\alpha$  increases from 0 to 4.

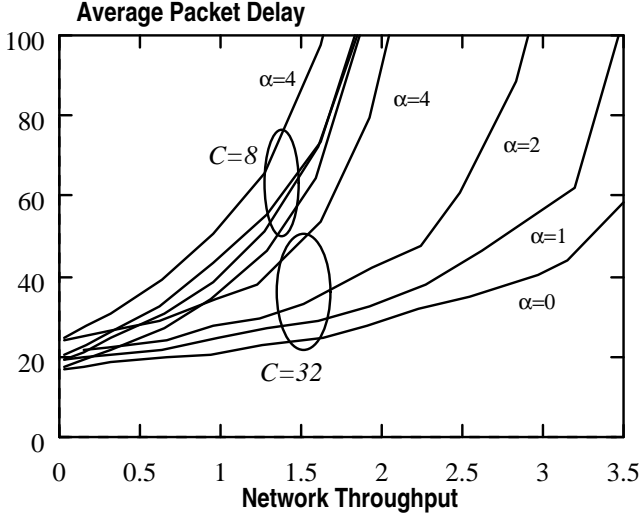


Figure 7: Performance of I-SA\* with varying  $\alpha$  for  $\alpha \in \{0, 1, 2, 4\}$ ,  $M = 32$ ,  $l = 16$ ,  $A = 16$  and  $W = 1$ .

**Varying Window Size:** In order to diminish the impact of propagation delay and processing latency, a window of packets may be transmitted after tuning to a channel as explained in Section 2.1.4. The effect of varying window size with respect to varying  $a$  and  $\alpha$  is shown in Fig. 8 for  $C = 16$ ,  $M = 32$ ,  $\alpha \in \{0, 1, 2, 4\}$ ,  $a \in \{2, 8\}$ . For each combination of  $a$  and  $\alpha$ ,  $\mathcal{D}$  at  $\mathcal{S} = 2.3$  has been plotted. Transmitting a window of packets reduces the propagation delay sensitivity of the acknowledgment since more than one packet can be acknowledged at the same time, and also reduces the impact of processing latency  $\alpha$ . The graph verifies this trend showing that  $\mathcal{D}$  decreases with increasing  $W$  for all combinations of  $a$  and  $\alpha$ . For example,  $\mathcal{D}$  at  $\mathcal{S} = 2.3$  for  $C = 16$ ,  $M = 32$  and  $a = 0$  decreases by 20% when  $W$  is increased from 1 to 4. Increasing  $W$  beyond 4 did not show any significant improvement in performance.

### 3.4 Comparison of I-SA\* and I-TDMA\*

Fig. 9 compares the two protocols for  $M \in \{16, 32, 64\}$ ,  $C = M/2$ ,  $l = M/2$ ,  $A = M/2$  and varying  $\alpha$ . Only I-TDMA\*<sub>1</sub> is plotted when  $CT > M$  since I-TDMA\*<sub>1</sub> was shown in the previous section to have better performance than I-TDMA\*<sub>2</sub> for  $C < M$ .

I-SA\* can offer lower delay under light input traffic but the values herein chosen for  $l$  and  $A$  result in higher delay. Delay is not dependent on  $C$  or  $M$  under light traffic but is determined by  $l$  and  $A$ . I-TDMA\* is sensitive to  $C$ ,  $M$  and  $\alpha$  since cycle length  $\mathcal{L}$  depends on the allocation scheme and average packet delay is proportional to cycle length. As the load increases, I-SA\* collapses because of increased collisions and is not able to withstand heavy traffic. On the other hand, I-TDMA\* does not collapse under heavy traffic and provides higher throughput.

The maximum theoretical throughput per channel for I-SA\* is 0.36 which is not attained because of finite population and explicit acknowledgment requirements. I-TDMA\* is more robust at higher loads and its saturation point is higher than that of I-SA\* for all values of  $\alpha$  irrespective of the allocation scheme used. If  $CT \leq M$ , I-TDMA\* offers the maximum theoretical throughput of  $C$  achieved with  $C$  multi-access channels. Both protocols are

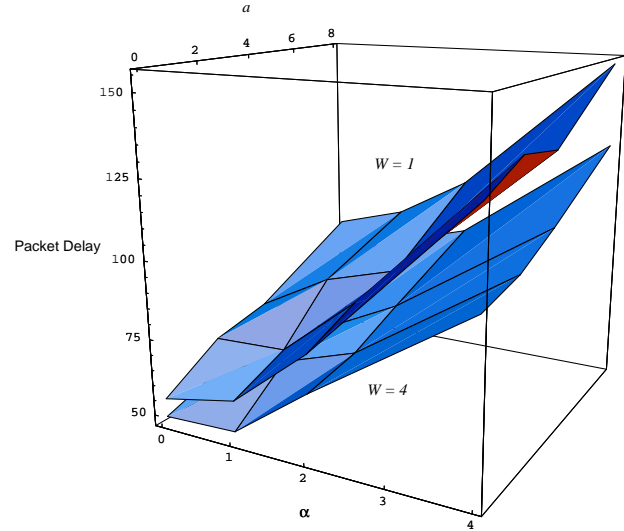


Figure 8: Performance of I-SA\* with varying  $W$  for  $C = 16$ ,  $M = 32$ ,  $a \in \{0, 2, 8\}$ ,  $\alpha \in \{0, 1, 2, 4\}$ ,  $l = 16$ ,  $A = 16$  and  $W \in \{1, 4\}$ .  $\mathcal{D}$  at  $\mathcal{S} = 2.3$  has been plotted for all combinations.

able to take advantage of an increase in the number of channels. However, the impact of increased switching overhead for large  $C$  is significant in both cases. The impact is higher in I-TDMA\*<sub>1</sub> where the cycle length is equal to  $CT$ .

For  $\alpha = 0$ ,  $\mathcal{S}_{max}$  offered by I-TDMA\* is higher than I-SA\* by 330% for  $M = 16$  and 430% for  $M = 64$  where  $C = M/2$  in both cases. The increase in maximum throughput diminishes with increasing  $\alpha$ . For  $\alpha = 2$ , I-TDMA\*<sub>0</sub> cannot be used since  $CT > M$ . I-TDMA\*<sub>1</sub> offers a maximum throughput of  $M/T$ . The increase in  $\mathcal{S}_{max}$  from I-SA\* is 270% with I-TDMA\*<sub>1</sub> for  $\alpha = 2$ ,  $M \in \{16, 32, 64\}$  and  $C = M/2$ .

The principal advantage of I-TDMA\* over I-SA\* is its insensitivity to propagation delay. I-SA\* is dependent on acknowledgments and its performance reduces significantly as  $a$  increases. I-TDMA\* offers better throughput than I-SA\* but its main drawback is the dependence of cycle length on  $M$  ( $C$  and  $\alpha$  in I-TDMA\*<sub>1</sub>) which results in increased delay. I-SA\* has the capability to offer lower delay under light traffic. As traffic intensity increases, I-TDMA\* is clearly the better choice due to stability and higher network throughput.

## 4 CONCLUSIONS

This paper analyzed the performance of two pre-allocation based media access protocols for a WDM star-coupled photonic network. The network architecture considered has nodes with one tunable transmitter and one fixed receiver. Each node in the system has a preassigned home channel to receive data packets. This paper considered both a random and static approach to access arbitration. Detailed discrete-event based simulation results were used to study the protocol behavior. I-SA\* was shown to have lower packet delay at lighter loads compared to I-TDMA\*. However, the performance of I-TDMA\* under heavy traffic is superior to that of I-SA\* since its saturation point is higher. I-TDMA\* is more sensitive to increase in system size. I-SA\* is sensitive to propagation delay because it requires acknowledgments unlike I-TDMA\*.

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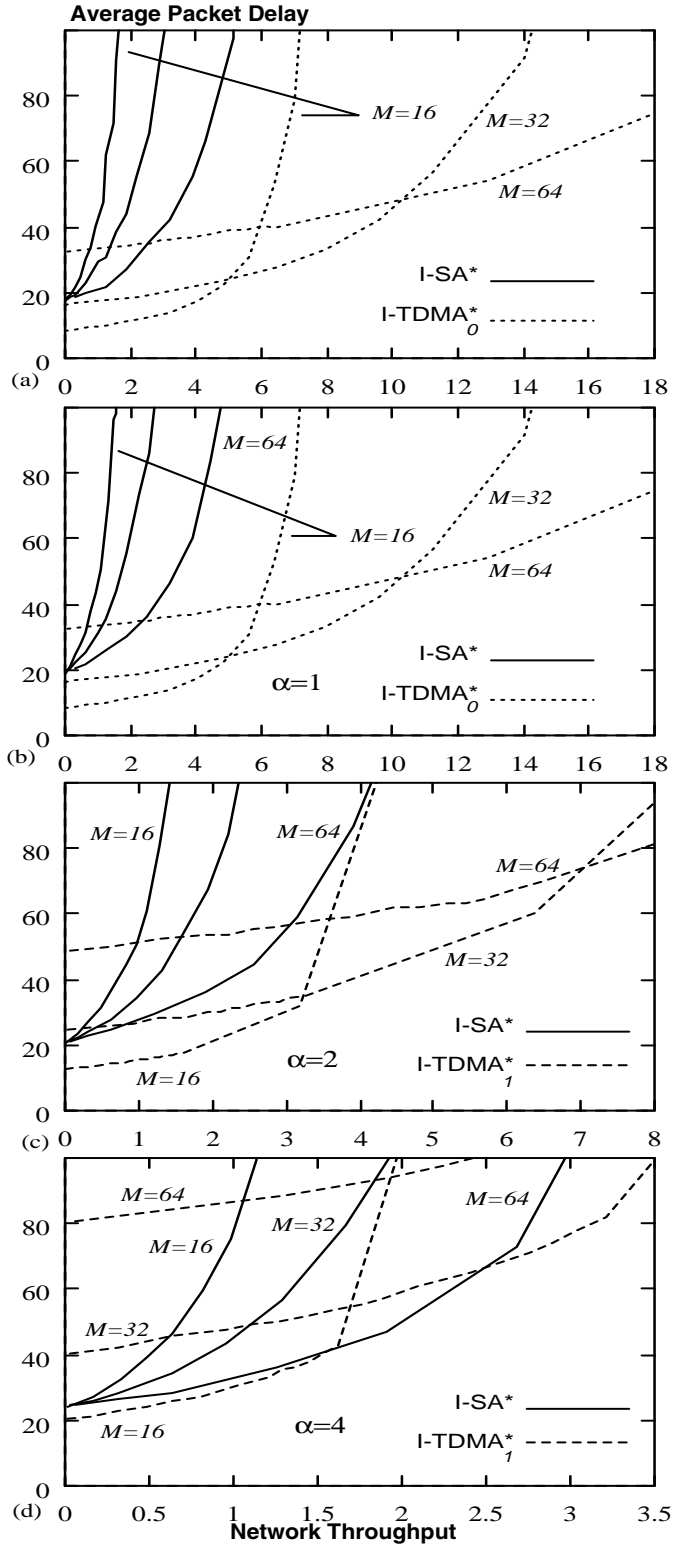


Figure 9: Comparison of I-SA\* and I-TDMA\* for  $M \in \{16, 32, 64\}$ ,  $C = M/2$ ,  $l = M/2$ ,  $A = M/2$  and  $W = 1$ : (a)  $\alpha = 0$  (b)  $\alpha = 1$  (c)  $\alpha = 2$  (d)  $\alpha = 4$ .